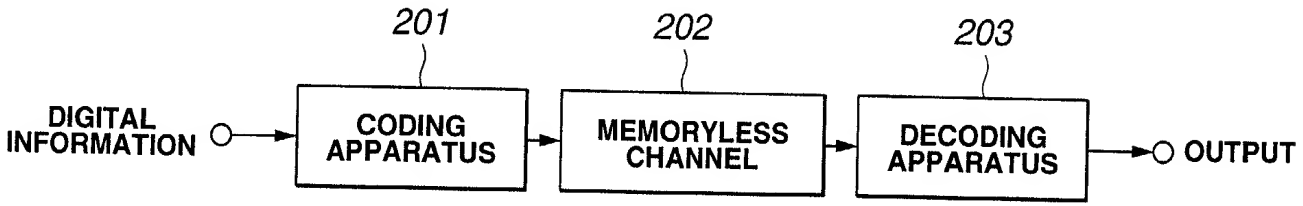
201
202
203
DIGITAL INFORMATION
CODING APPARATUS
MEMORYLESS CHANNEL
DECODING APPARATUS
OUTPUT

FIG.1

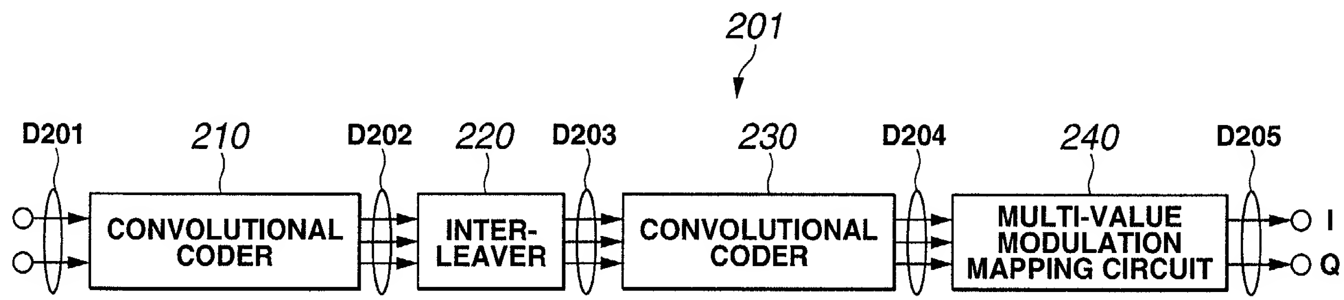
201
D201
210
CONVOLUTIONAL CODER
D202
220
INTER-LEAVER
D203
230
CONVOLUTIONAL CODER
D204
240
MULTI-VALUE MODULATION MAPPING CIRCUIT
D205
I
Q

FIG.2

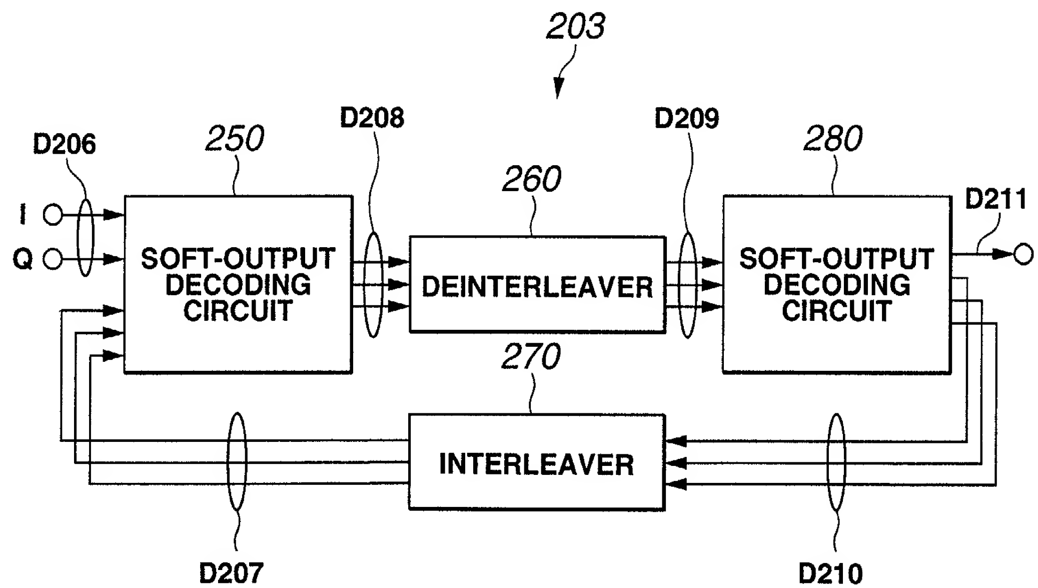
203
D206
I
Q
250
SOFT-OUTPUT DECODING CIRCUIT
D208
260
DEINTERLEAVER
D209
280
SOFT-OUTPUT DECODING CIRCUIT
D211
270
INTERLEAVER
D207
D210

FIG.3

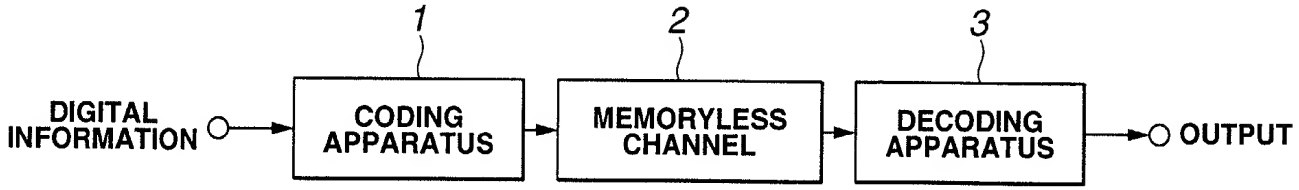
1
2
3
DIGITAL INFORMATION
CODING APPARATUS
MEMORYLESS CHANNEL
DECODING APPARATUS
OUTPUT

FIG.4

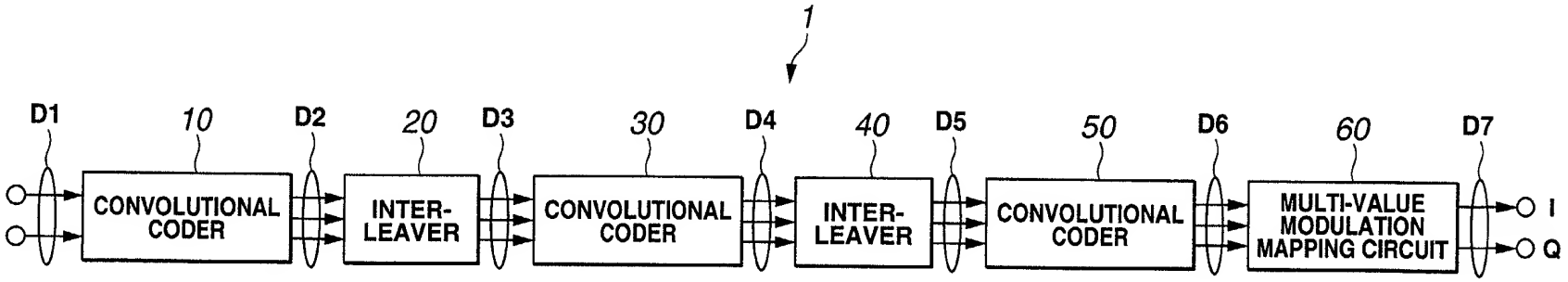
1
D1
10
D2
20
D3
30
D4
40
D5
50
D6
60
D7
CONVOLUTIONAL CODER
INTER-LEAVER
CONVOLUTIONAL CODER
INTER-LEAVER
CONVOLUTIONAL CODER
MULTI-VALUE MODULATION MAPPING CIRCUIT
I
Q

FIG.5

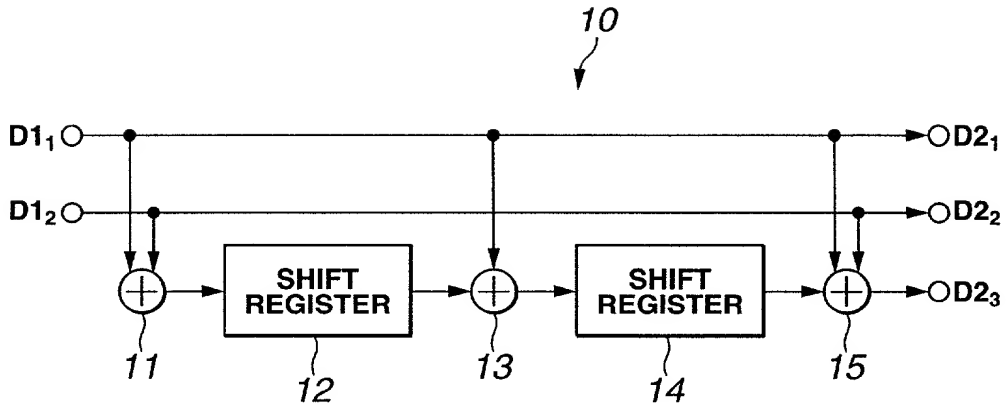
10
D1₁
D1₂
D2₁
D2₂
D2₃
SHIFT REGISTER
SHIFT REGISTER
11
12
13
14
15

FIG.6

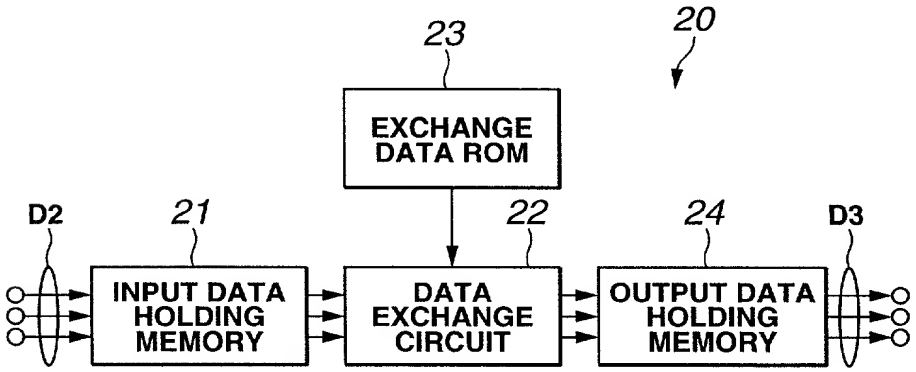
23
20
EXCHANGE DATA ROM
D2
21
22
24
D3
INPUT DATA HOLDING MEMORY
DATA EXCHANGE CIRCUIT
OUTPUT DATA HOLDING MEMORY

FIG.7

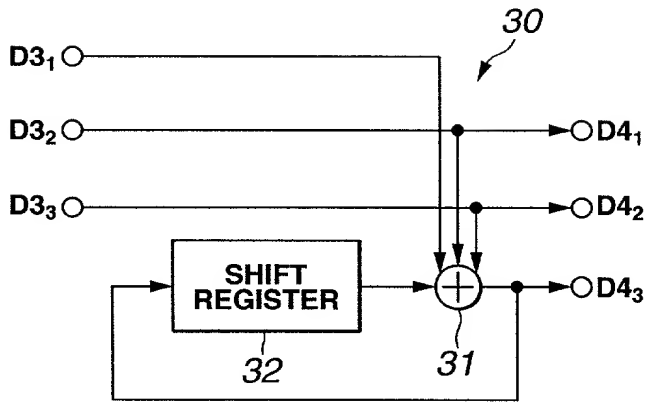

FIG.8

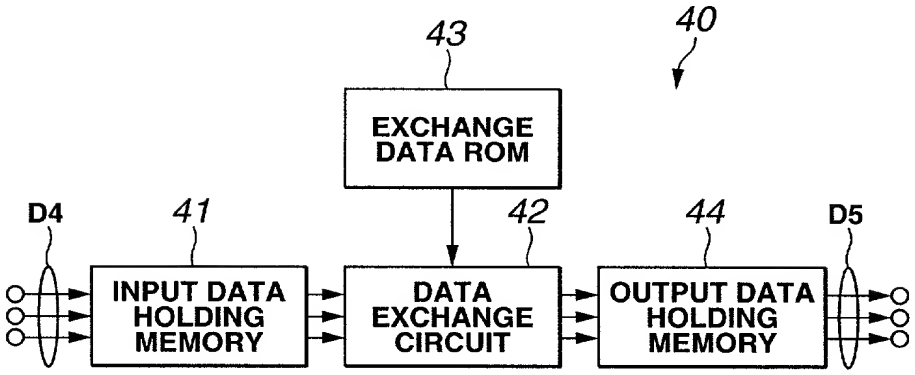

FIG.9

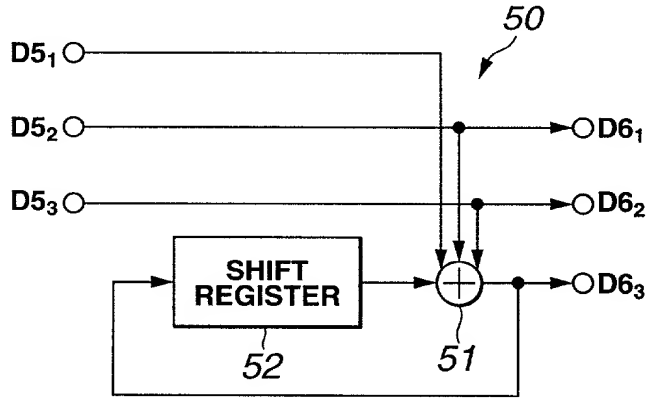

FIG.10

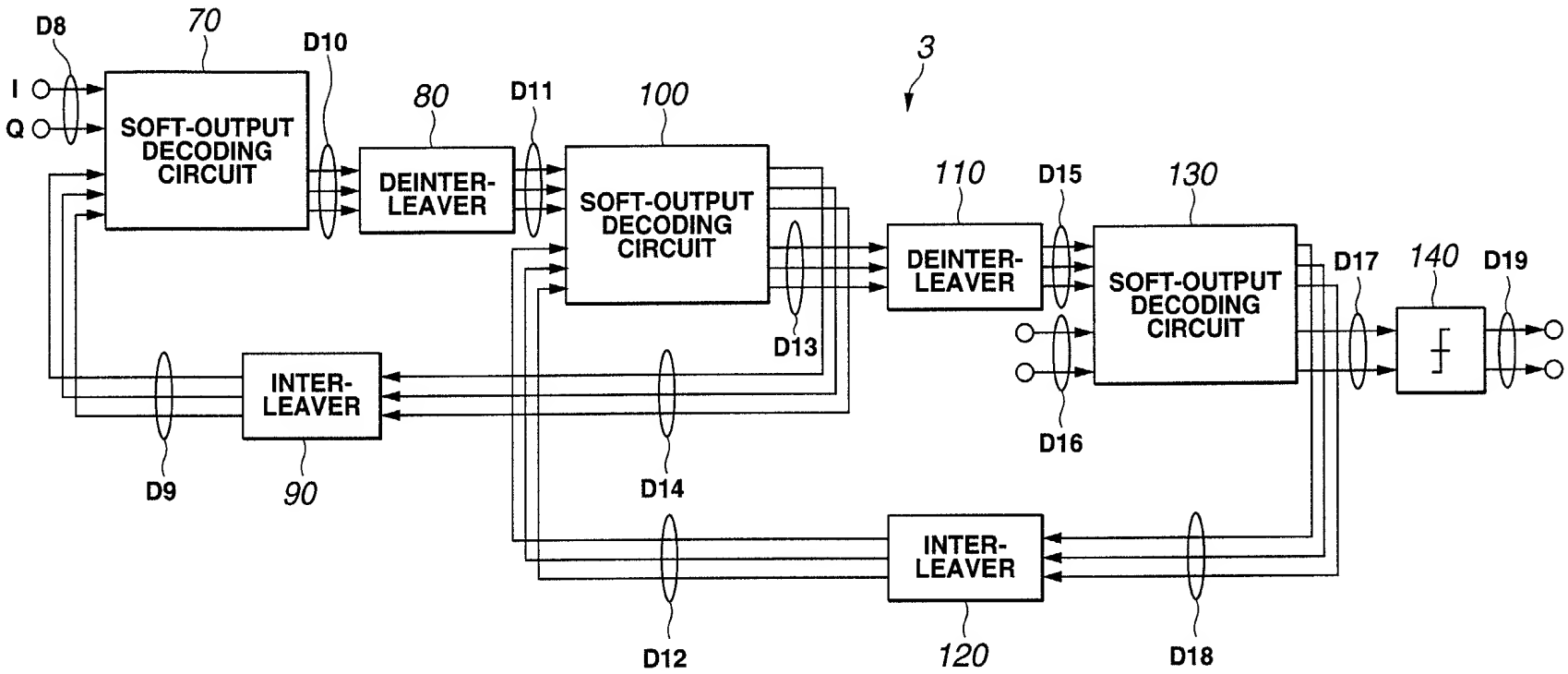

FIG.11

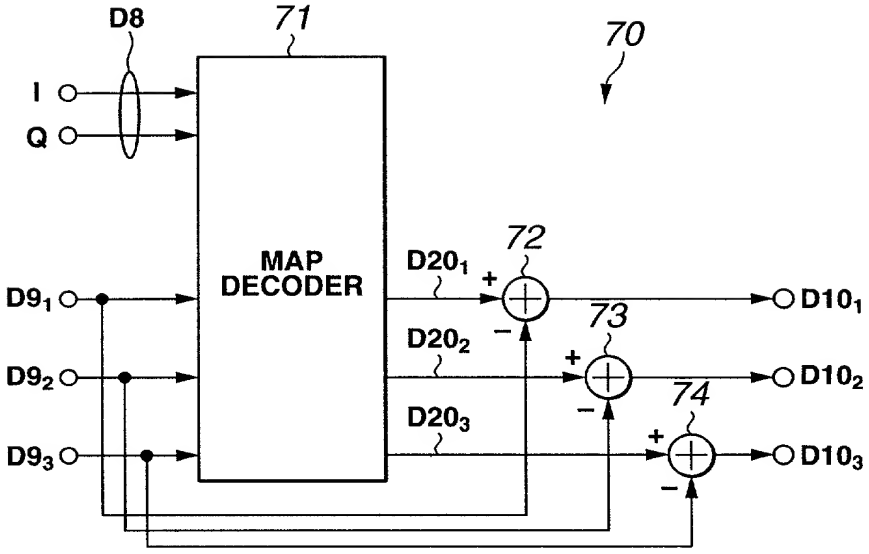
D8
71
70
I
Q
MAP
DECODER
D20₁
D20₂
D20₃
72
73
74
+
−
D9₁
D9₂
D9₃
D10₁
D10₂
D10₃

FIG.12

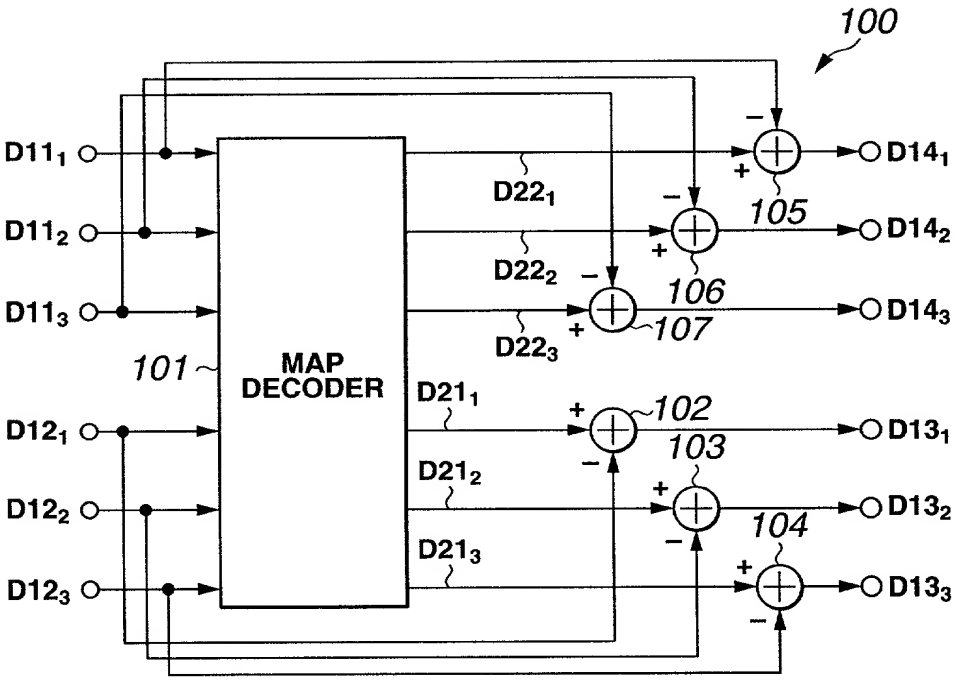
100
D11₁
D11₂
D11₃
101
MAP DECODER
D12₁
D12₂
D12₃
D22₁
D22₂
D22₃
D21₁
D21₂
D21₃
105
106
107
102
103
104
D14₁
D14₂
D14₃
D13₁
D13₂
D13₃

FIG.13

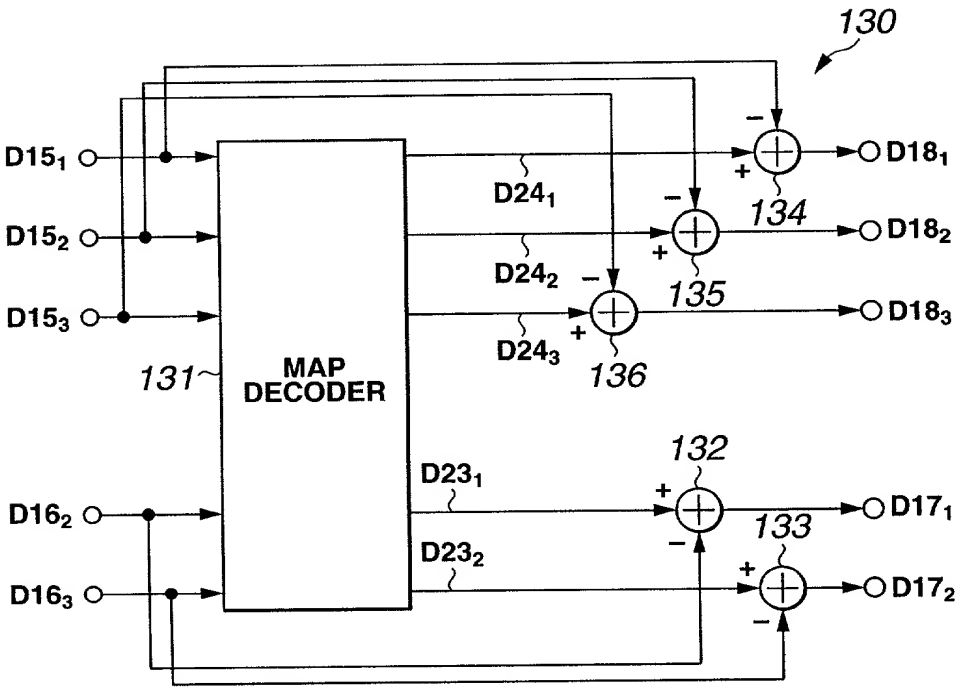
130
D15$_1$
D15$_2$
D15$_3$
131
MAP DECODER
D24$_1$
D24$_2$
D24$_3$
134
135
136
D18$_1$
D18$_2$
D18$_3$
D16$_2$
D16$_3$
D23$_1$
D23$_2$
132
133
D17$_1$
D17$_2$

FIG.14

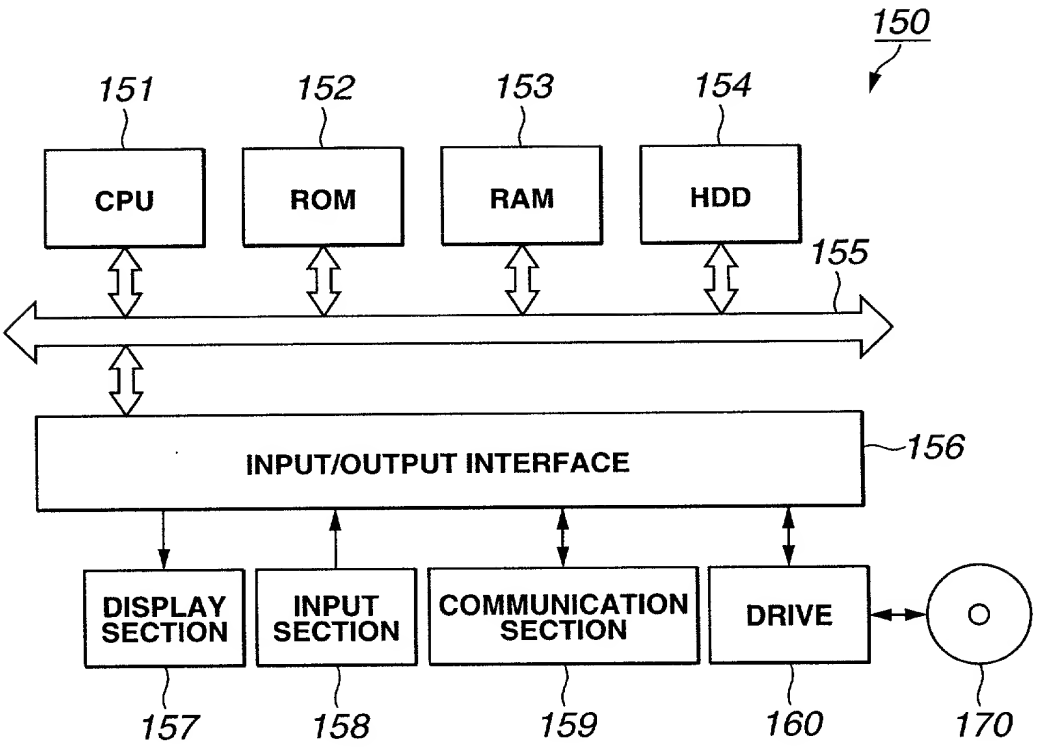
150
151
152
153
154
CPU
ROM
RAM
HDD
155
INPUT/OUTPUT INTERFACE
156
DISPLAY SECTION
INPUT SECTION
COMMUNICATION SECTION
DRIVE
157
158
159
160
170

FIG.15